

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 07 and 08. Add \overline{SEM} condition to V_{DR} and I_{CC6} in table I. Add footnote <u>2/</u> to semaphore truth table on sheet 15. Add footnote <u>2/</u> to interrupt flag truth table on sheet 16. Add note <u>2/</u> to sheet 17. Add \overline{SEM} and note 9 on sheet 20. Update boilerplate. Editorial changes throughout.	96-10-10	Ray Monnin

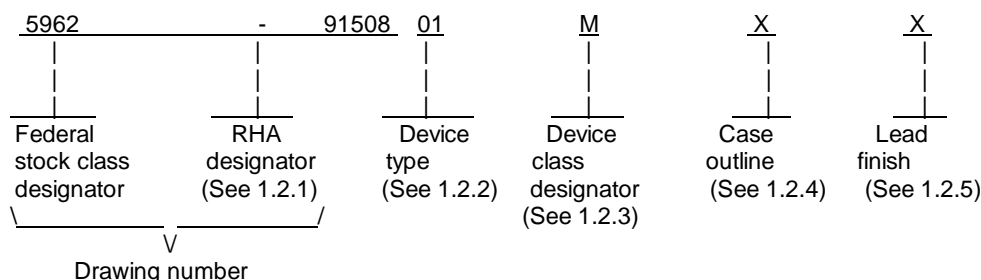
REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				
REV STATUS OF SHEETS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Jeff Bowling	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216			
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 16K X 8 DUAL PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON			
	APPROVED BY Michael A. Frye				
	DRAWING APPROVAL DATE 93-04-15				
	REVISION LEVEL A	SIZE A	CAGE CODE 67268	5962-91508	
		SHEET 1 OF 30			

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Data retention</u>	<u>Access time</u>
01	7006	16k X 8 Dual Port Static RAM	No	70ns
02	7006	16k X 8 Dual Port Static RAM	Yes	70ns
03	7006	16k X 8 Dual Port Static RAM	No	55ns
04	7006	16k X 8 Dual Port Static RAM	Yes	55ns
05	7006	16k X 8 Dual Port Static RAM	No	45ns
06	7006	16k X 8 Dual Port Static RAM	Yes	45ns
07	7006	16k X 8 Dual Port Static RAM	No	35ns
08	7006	16k X 8 Dual Port Static RAM	Yes	35ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CMGA3-PN	68	pin grid array
Y	See figure 1	68	flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65° C to +150° C
DC output current	50 mA
Maximum power dissipation (P_D)	2.2 W
Lead temperature (soldering, 10 seconds)	260° C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	20° C/W
Maximum junction temperature (T_J)	+150° C 3/
DC input voltage range	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
DC output voltage range	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/
Output voltage applied in high Z state	-0.5 V dc to $V_{CC} + 0.5$ V dc

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
High level input voltage (V_{IH})	+2.2 V dc to +6.0 V dc
Low level input voltage (V_{IL}) 2/	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55° C to +125° C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to GND unless otherwise specified.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.
5/ When a QML source exists, a value shall be provided.

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(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

- c. Interim and final electrical parameters shall be as specified in table IIA herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 4 mA V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	All		0.4	V
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -4 mA V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	All	2.4		V
Input leakage current 1/	I _{LI}	V _{CC} = 5.5 V, V _{IN} = 0 V to V _{CC}	1, 2, 3	01,03, 05,07		10	μA
				02,04, 06,08		5	
Output leakage current	I _{LO}	V _{CC} = 5.5 V, C _E = V _{IH} , V _{OUT} = 0 V to V _{CC}	1, 2, 3	01,03, 05,07		10	μA
				02,04, 06,08		5	
Dynamic operating current (both ports active)	I _{CC1}	V _{CC} = 5.5 V, C _E ≤ V _{IL} , Outputs open, SEM ≥ V _{IH} , f = f _{MAX} 2/	1, 2, 3	01		390	mA
				02		330	
				03		395	
				04		335	
				05		400	
				06		340	
				07		300	
				08		250	
Standby current (both ports - TTL level inputs)	I _{CC2}	V _{CC} = 5.5 V, C _{ER} = C _{EL} ≥ V _{IH} , SEM _R = SEM _L ≥ V _{IH} , f = f _{MAX} 2/	1, 2, 3	01,03, 05,07		85	mA
				02,04, 06,08		65	
Standby current (one port - TTL level inputs)	I _{CC3}	V _{CC} = 5.5 V, C _{EL} or C _{ER} ≥ V _{IH} , active port outputs open, f = f _{MAX} 2/, SEM _R = SEM _L ≥ V _{IH}	1, 2, 3	01,03, 05,07		290	mA
				02,04, 06,08		250	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Full standby current (both ports - all CMOS level inputs)	I _{CC4}	V _{CC} = 5.5 V, Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0 Hz <u>3/</u> , SEM _R = SEM _L ≥ V _{CC} - 0.2 V	1, 2, 3	01,03, 05,07		30	mA
				02,04, 06,08		10	
Full standby current (one port - all CMOS level inputs)	I _{CC5}	V _{CC} = 5.5 V, One Port \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2$ V, SEM _R = SEM _L ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, active port outputs open, f = f _{MAX} <u>2/</u>	1, 2, 3	01,03, 05,07		260	mA
				02,04, 06,08		215	
Data retention voltage	V _{DR}	V _{CC} = 2.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or ≤ 0.2 V, SEM _L ≥ V _{CC} - 0.2 V	1, 2, 3	02,04, 06,08	2.0		V
Data retention current	I _{CC6}		1, 2, 3	02,04, 06,08		4	mA
Input capacitance	C _{IN}	V _{IN} = 0.0 V, V _{CC} = 5.0 V, f = 1 MHz, T _A = 25°C, see 4.4.1e	4	All		11	pF
Output capacitance	C _{OUT}	V _{OUT} = 0.0 V, V _{CC} = 5.0 V, f = 1 MHz, T _A = 25°C, see 4.4.1e	4	All		11	pF
Functional testing		See 4.4.1c	7,8A, 8B	All			
Chip deselect to data retention time <u>5/</u>	t _{CDR}	V _{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or ≤ 0.2 V see figures 4 and 5 <u>6/</u>	9, 10, 11	02,04, 06,08	0		ns
Operation recovery time <u>5/</u>	t _R		9, 10, 11	02,04, 06,08	t _{AVAV}		ns
Read cycle time	t _{AVAV}	See figures 4 and 5 <u>6/</u>	9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ TC ≤ +125°C 4.5 V ≤ VCC ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address access time	tAVQV	See figures 4 and 5 <u>6/</u>	9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
Chip enable access time <u>7/</u>	tELQV		9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
Output enable access time	tOLQV		9, 10, 11	01,02		35	ns
				03,04		30	
				05-08		25	
Output hold from address change	tAVQX		9, 10, 11	All	3		ns
Output enable to output active <u>5/</u>	tOLQX	See figures 4 and 5 <u>8/</u>	9, 10, 11	All	5		ns
Output disable to output inactive <u>5/</u>	tOHQZ		9, 10, 11	01,02		30	ns
				03,04		25	
				05,06		20	
				07,08		15	
Chip enable to power up time <u>5/</u>	tELPU	See figures 4 and 5 <u>6/</u>	9, 10, 11	All	0		ns
Chip disable to power down time <u>5/</u>	tEHPD		9, 10, 11	All		50	ns
Semaphore flag update pulse (OE or SEM)	tSOP		9, 10, 11	All	15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t _{AVAV}	See figures 4 and 5 <u>6/</u>	9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		
Chip enable to end of write <u>9/</u>	t _{ELWH}		9, 10, 11	01,02	50		ns
				03,04	45		
				05,06	40		
				07,08	30		
Address valid to end of write	t _{AVWH}		9, 10, 11	01,02	50		ns
				03,04	45		
				05,06	40		
				07,08	30		
Address set-up time <u>9/</u>	t _{AVWL}	9, 10, 11	All	0		ns	
Write pulse width	t _{WLWH}	9, 10, 11	01,02	50		ns	
			03,04	40			
			05,06	35			
			07,08	30			
Write recovery time	t _{WHAX}	9, 10, 11	All	0		ns	
Data valid to end of write	t _{DVWH}	9, 10, 11	01,02	40		ns	
			03,04	30			
			05,06	25			
			07,08	20			
Data hold time <u>10/</u>	t _{WHDX}	9, 10, 11	All	0		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write enable to output inactive	t _{WLQZ}	See figures 4 and 5 <u>5/ 8/</u>	9, 10, 11	01,02		30	ns
				03,04		25	
				05,06		20	
				07,08		15	
Output active from end of write <u>10/</u>	t _{WHQX}		9, 10, 11	All	0		ns
$\overline{\text{SEM}}$ flag write to read time	t _{SWRD}	See figures 4 and 5 <u>6/</u>	9, 10, 11	All	10		ns
$\overline{\text{SEM}}$ flag contention window	t _{SPS}		9, 10, 11	All	10		ns
$\overline{\text{BUSY}}$ access time from address match	t _{BAA}	M/ $\overline{\text{S}}$ = H See figures 4 and 5 <u>6/</u>	9, 10, 11	01-04		45	ns
				05,06		35	
				07,08		20	
$\overline{\text{BUSY}}$ disable time from address not matched	t _{BDA}		9, 10, 11	01-04		40	ns
				05-08		30	
$\overline{\text{BUSY}}$ access time from chip enable low	t _{BAC}		9, 10, 11	01-04		40	ns
				05,06		30	
				07,08		20	
$\overline{\text{BUSY}}$ disable time from chip enable high	t _{BDC}		9, 10, 11	01-04		35	ns
				05,06		25	
				07,08		20	
Arbitration priority set- up time <u>11/</u>	t _{APS}		9, 10, 11	All	5		ns
$\overline{\text{BUSY}}$ disable to valid data <u>12/</u>	t _{BDD}		9, 10, 11	All		<u>12/</u>	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{BUSY}}$ input to write <u>13/</u>	t _{WB}	M/ $\overline{\text{S}}$ = L See figures 4 and 5 <u>6/</u>	9, 10, 11	All	0		ns
Write hold after $\overline{\text{BUSY}}$ <u>14/</u>	t _{WH}		9, 10, 11	All	25		ns
Write pulse to data delay	t _{WDD}	See figures 4 and 5 <u>6/</u>	9, 10, 11	01,02		95	ns
				03,04		80	
				05,06		70	
				07,08		60	
Write data valid to read data delay	t _{DDD}		9, 10, 11	01,02		80	ns
				03,04		65	
				05,06		55	
				07,08		45	
Interrupt set time	t _{INS}		9, 10, 11	01,02		50	ns
				03,04		40	
				05-08		35	
Interrupt reset time	t _{INR}		9, 10, 11	01,02		50	ns
				03,04		40	
				05-08		35	

1/ At V_{CC} ≤ 2.0 V input leakages are undefined.

2/ At f_{MAX}, address and data inputs (except OE) are cycling at the maximum frequency of read cycle of 1/t_{AVAV}, and using AC test conditions of input levels of GND to 3 V.

3/ f = 0 Hz means no address or control lines change.

4/ H = logic "1" state, L = logic "0" state.

5/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

6/ AC measurements assume transition times ≤ 5 ns, input levels from ground to 3.0 V, timing reference levels of 1.5 V, and the output load in figure 4, circuit A.

7/ To access RAM: CE = L, SEM = H.

8/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 4, circuit B.

9/ To access RAM, CE = L, SEM = H. To access Semaphore, CE = H, SEM = L. Either condition must be valid for the entire t_{ELWH} time.

10/ The specification for t_{WHDX} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{WHDX} and t_{WHQX} values will vary over voltage and temperature, the actual t_{WHDX} will always be smaller than the actual t_{WHQX}.

11/ To ensure that the earlier of the two ports wins.

12/ t_{BDD} is a calculated parameter and is greater of 0 ns, t_{WDD} - t_{DVWH}(actual) or t_{WDD} - t_{WLWH}(actual).

13/ To ensure that the write cycle is inhibited during contention.

14/ To ensure that a write cycle is completed after contention.

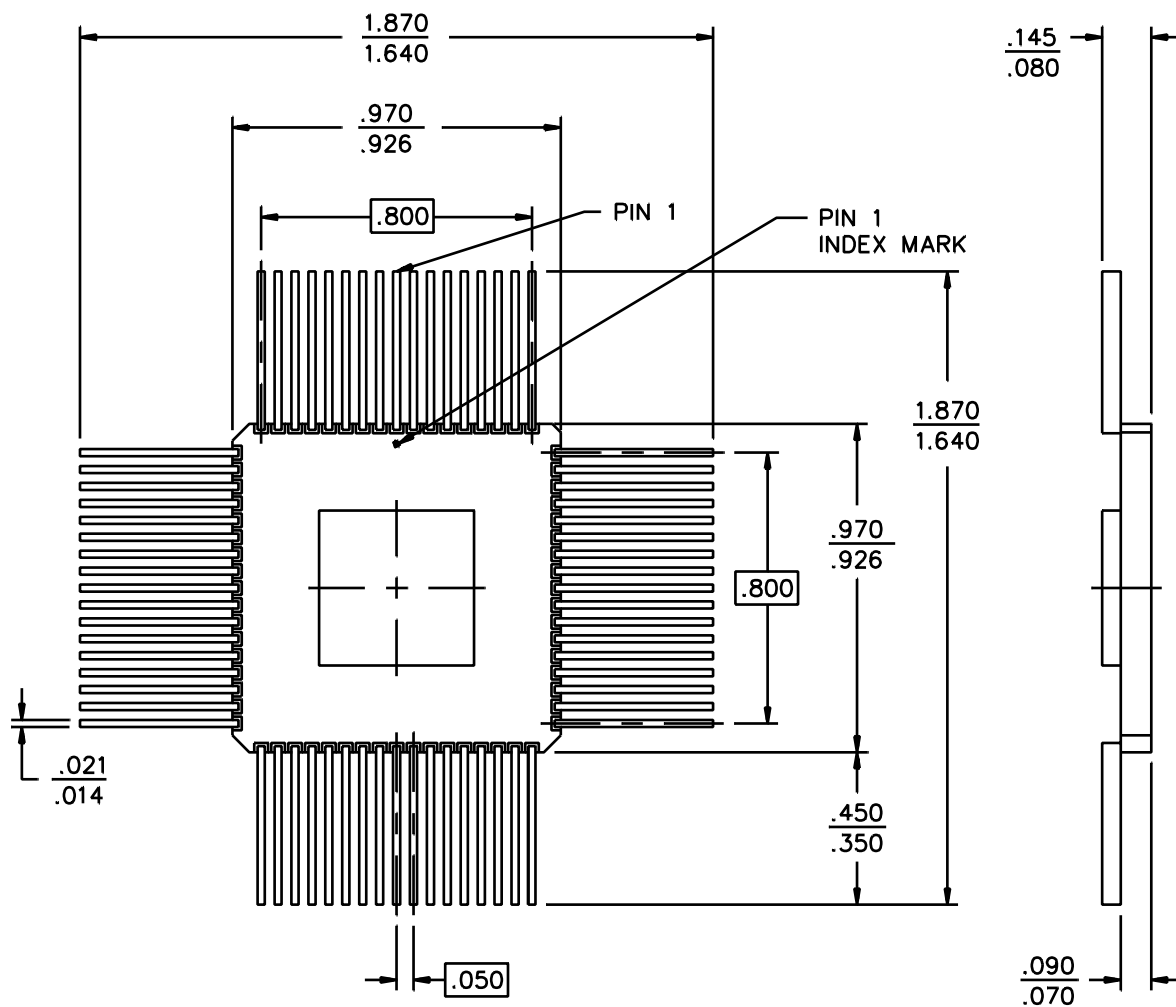
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Notes:

1. All dimensions are in inches.
2. BSC - Basic lead spacing between centers (boxed measurements indicate BSC dimensions).

<u>Inches</u>	<u>Millimeters</u>	<u>Inches</u>	<u>Millimeters</u>
.014	.36	.350	8.89
.021	.53	.450	11.43
.050	1.27	.800	20.32
.070	1.78	.926	23.52
.080	2.03	.970	24.64
.090	2.29	1.640	41.66
.145	3.68	1.870	47.50

FIGURE 1. Case outline.

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Device types	All		
Case outline	X		
Terminal number	1/ 2/ Terminal symbol	Terminal number	1/ 2/ Terminal symbol
A2	I/O _{1L}	F10	GND
A3	I/O _{0L}	F11	BUSY _L
A4	OE _L	G1	I/O _{2R}
A5	SEM _L	G2	I/O _{1R}
A6	NC	G10	BUSY _R
A7	V _{CC}	G11	M/S
A8	A _{11L}	H1	I/O _{3R}
A9	A _{9L}	H2	V _{CC}
A10	A _{7L}	H10	A _{0R}
B1	I/O _{3L}	H11	INT _R
B2	I/O _{2L}	J1	I/O _{5R}
B3	NC	J2	I/O _{4R}
B4	R/W _L	J10	A _{2R}
B5	CE _L	J11	A _{1R}
B6	A _{13L}	K1	I/O _{6R}
B7	A _{12L}	K2	I/O _{7R}
B8	A _{10L}	K3	OE _R
B9	A _{8L}	K4	SEM _R
B10	A _{6L}	K5	NC
B11	A _{5L}	K6	GND
C1	I/O _{5L}	K7	A _{11R}
C2	I/O _{4L}	K8	A _{9R}
C10	A _{3L}	K9	A _{7R}
C11	A _{4L}	K10	A _{4R}
D1	I/O _{6L}	K11	A _{3R}
D2	GND	L2	NC
D10	A _{1L}	L3	R/W _R
D11	A _{2L}	L4	CE _R
E1	V _{CC}	L5	A _{13R}
E2	I/O _{7L}	L6	A _{12R}
E10	INT _L	L7	A _{10R}
E11	A _{0L}	L8	A _{8R}
F1	I/O _{0R}	L9	A _{6R}
F2	GND	L10	A _{5R}

- 1/ All V_{CC} pins must be connected to power supply.
2/ All GND pins must be connected to ground supply.

FIGURE 2. Terminal connections.

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Device types	All		
Case outline	Y		
Terminal number	1/ 2/ Terminal symbol	Terminal number	1/ 2/ Terminal symbol
1	A _{13L}	35	GND
2	NC	36	A _{12R}
3	CE _L	37	A _{11R}
4	SEM _L	38	A _{10R}
5	R/W _L	39	A _{9R}
6	OE _L	40	A _{8R}
7	NC	41	A _{7R}
8	I/O _{0L}	42	A _{6R}
9	I/O _{1L}	43	A _{5R}
10	I/O _{2L}	44	A _{4R}
11	I/O _{3L}	45	A _{3R}
12	I/O _{4L}	46	A _{2R}
13	I/O _{5L}	47	A _{1R}
14	GND	48	A _{0R}
15	I/O _{6L}	49	INT _R
16	I/O _{7L}	50	BUSY _R
17	V _{CC}	51	M/S
18	GND	52	GND
19	I/O _{0R}	53	BUSY _L
20	I/O _{1R}	54	INT _L
21	I/O _{2R}	55	A _{0L}
22	V _{CC}	56	A _{1L}
23	I/O _{3R}	57	A _{2L}
24	I/O _{4R}	58	A _{3L}
25	I/O _{5R}	59	A _{4L}
26	I/O _{6R}	60	A _{5L}
27	I/O _{7R}	61	A _{6L}
28	NC	62	A _{7L}
29	OE _R	63	A _{8L}
30	R/W _R	64	A _{9L}
31	SEM _R	65	A _{10L}
32	CE _R	66	A _{11L}
33	NC	67	A _{12L}
34	A _{13R}	68	V _{CC}

- 1/ All V_{CC} pins must be connected to power supply.
2/ All GND pins must be connected to ground supply.

FIGURE 2. Terminal connections - Continued.

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Non-contention read/write control 1/

Inputs <u>2/</u>				Outputs	Mode
\overline{CE}	R/ \overline{W}	\overline{OE}	\overline{SEM}	I/O ₀₋₇	
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATA _{IN}	Write to Memory
L	H	L	H	DATA _{OUT}	Read Memory
X	X	H	X	Hi-Z	Outputs Disabled

1/ H = logic "1" state, L = logic "0" state, X = "don't care" state, Hi-Z = high impedance state.

2/ A_{0L}-A_{13L} ≠ A_{0R}-A_{13R}

Semaphore read/write control 1/ 2/

Inputs				Outputs	Mode
\overline{CE}	R/ \overline{W}	\overline{OE}	\overline{SEM}	I/O ₀₋₇	
H	H	L	L	DATA _{OUT}	Read Data in Semaphore Flag
H	<u>3/</u>	X	L	DATA _{IN}	Write D _{IN0} into Semaphore Flag
L	X	X	L	-	Not Allowed

1/ H = logic "1" state, L = logic "0" state, X = "don't care" state.

2/ There are eight semaphore flags written to via I/O₀ and read from I/O₀ - I/O₁₅. These eight semaphores are addressed by A₀ - A₂.

3/ Rising edge of signal.

FIGURE 3. Truth tables.

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Interrupt flag 1/ 2/ 3/

Left Port					Right Port					Function
R/W _L	CE _L	OE _L	A0L-A13L	TNT _L	R/W _R	CE _R	OE _R	A0R-A13R	TNT _R	
L	L	X	3FFF	X	X	X	X	X	L <u>4/</u>	Set Right TNT _R Flag
X	X	X	X	X	X	L	L	3FFF	H <u>5/</u>	Reset Right TNT _R Flag
X	X	X	X	L <u>5/</u>	L	L	X	3FFE	X	Set Left TNT _L Flag
X	L	L	3FFE	H <u>4/</u>	X	X	X	X	X	Reset Left TNT _L Flag

1/ H = logic "1" state, L = logic "0" state, X = "don't care" state.

2/ TNT_R and TNT_L must be initialized at power-up.

3/ Assumes BUSY_L = BUSY_R = H.

4/ If BUSY_L = L, then no change.

5/ If BUSY_R = L, then no change.

Address busy arbitration 1/

Inputs			Outputs		Function
CE _L	CE _R	A0L-A13L A0R-A13R	BUSY _L <u>2/</u>	BUSY _R <u>2/</u>	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	<u>3/</u>	<u>3/</u>	Write Inhibit <u>4/</u>

1/ H = logic "1" state, L = logic "0" state, X = "don't care" state.

2/ BUSY_L and BUSY_R are both outputs when the part is configured as a master. Both are inputs when configured as a slave. BUSY_X outputs are push pull, not open drain outputs. On slaves the BUSY_X input internally inhibits writes.

3/ L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{AP5} is not met, either BUSY_L or BUSY_R = Low will result. BUSY_L or BUSY_R outputs cannot be low simultaneously.

4/ Writes to the left port are internally ignored when BUSY_L outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSY_R outputs are driving low regardless of actual logic level on the pin.

FIGURE 3. Truth tables - continued.

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Example of semaphore procurement sequence 1/ 2/

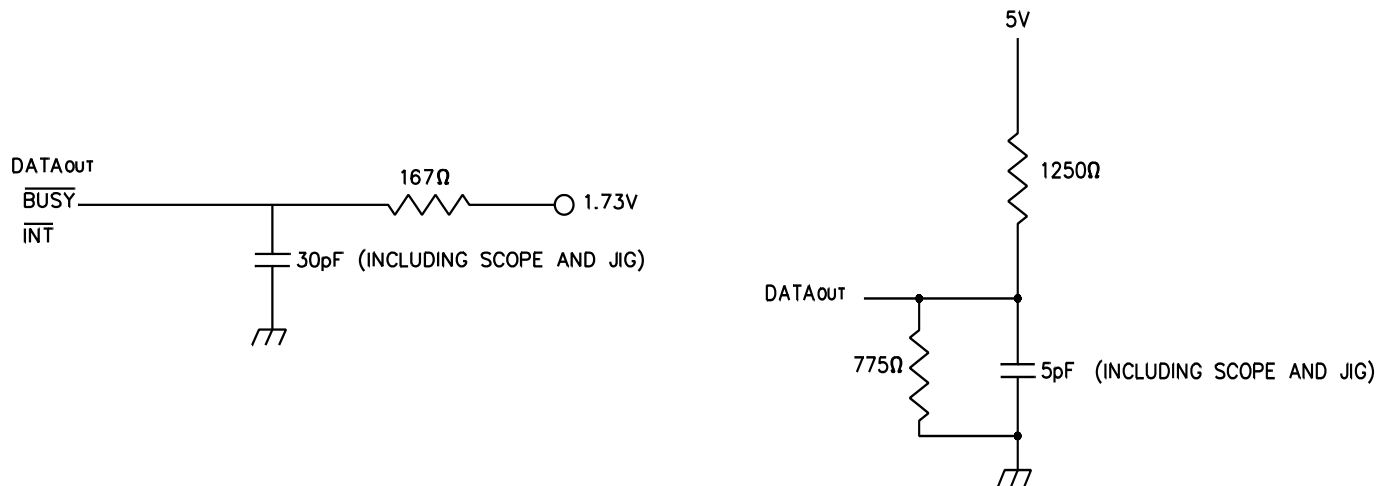
Functions	D ₀ -D ₇ Left	D ₀ -D ₇ Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

1/ This table denotes a sequence of events for only one of the eight semaphores.

2/ There are eight semaphore flags written to via I/O₀ and read from I/O₀ - I/O₁₅. These eight semaphores are addressed by A₀ - A₂.

FIGURE 3. Truth tables - continued.

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Circuit A

Circuit B (for t_{OLQX} , t_{OHQZ} , t_{WLQZ} and t_{WHQX})

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times (t_r , t_f)	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

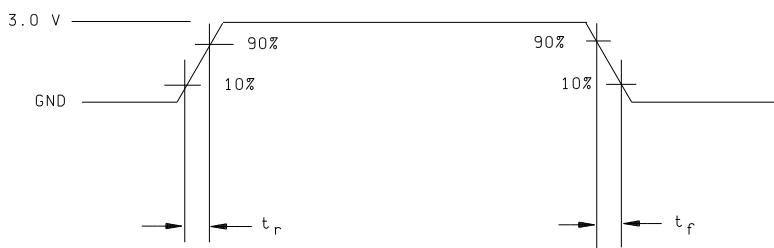


FIGURE 4. Output load circuits.

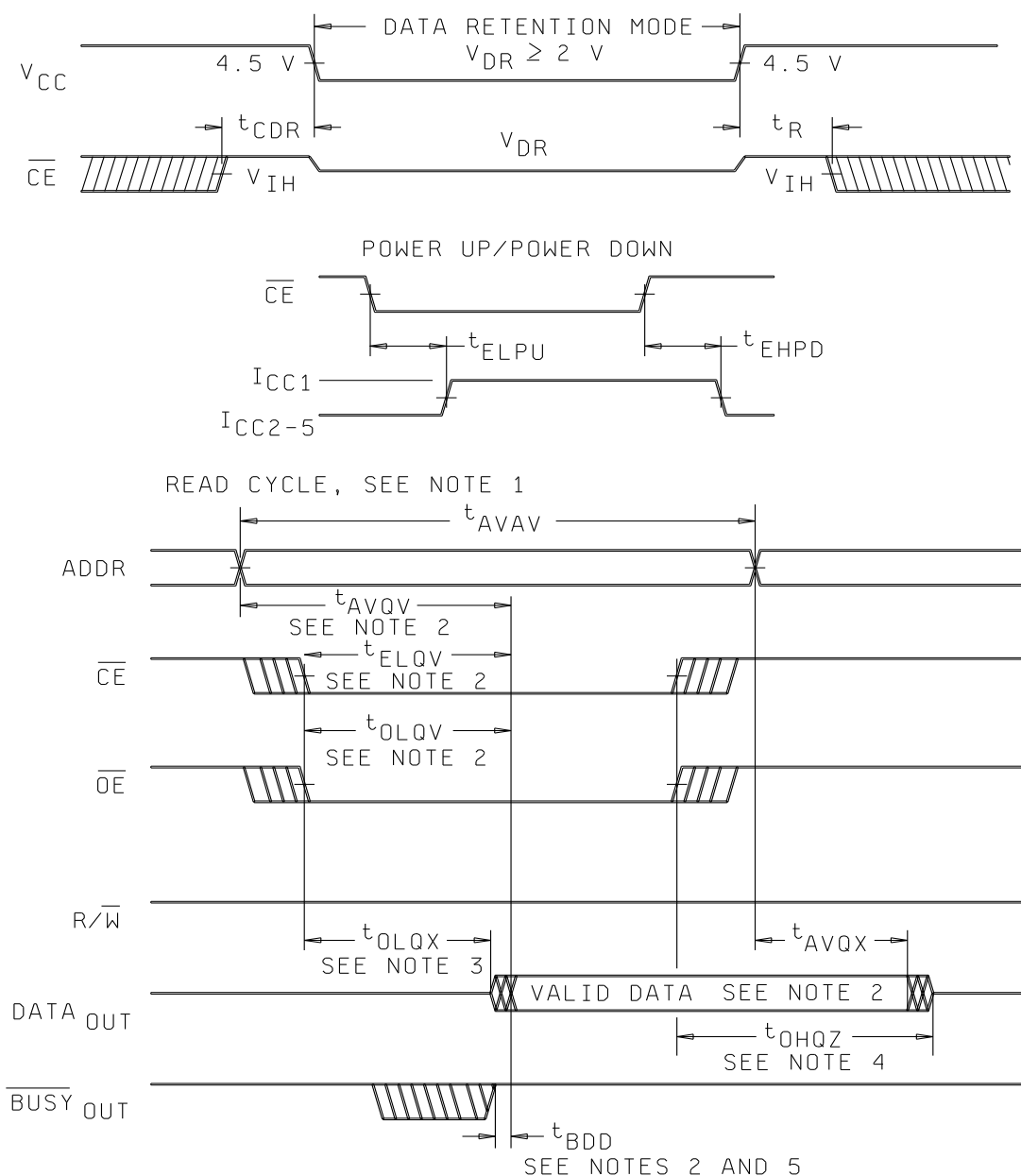
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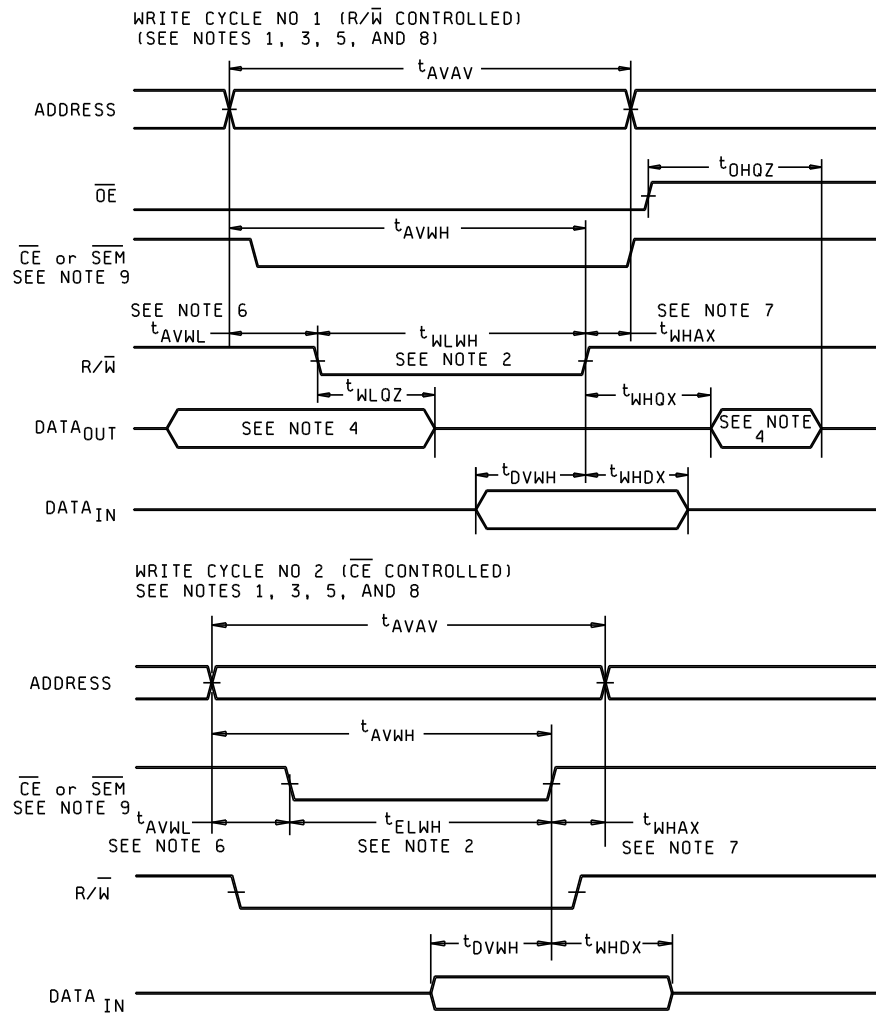


Notes on read operation:

1. $\overline{SEM} = H$.
2. Start of valid data depends on which timing becomes effective last, t_{OLQV} , t_{ELQV} , t_{AVQV} , t_{BDD} .
3. Timing depends on which signal is asserted last, \overline{OE} , \overline{CE} .
4. Timing depends on which signal is de-asserted first, \overline{OE} , \overline{CE} .
5. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $BUSY$ has no relation to valid output data.

FIGURE 5. Timing waveforms.

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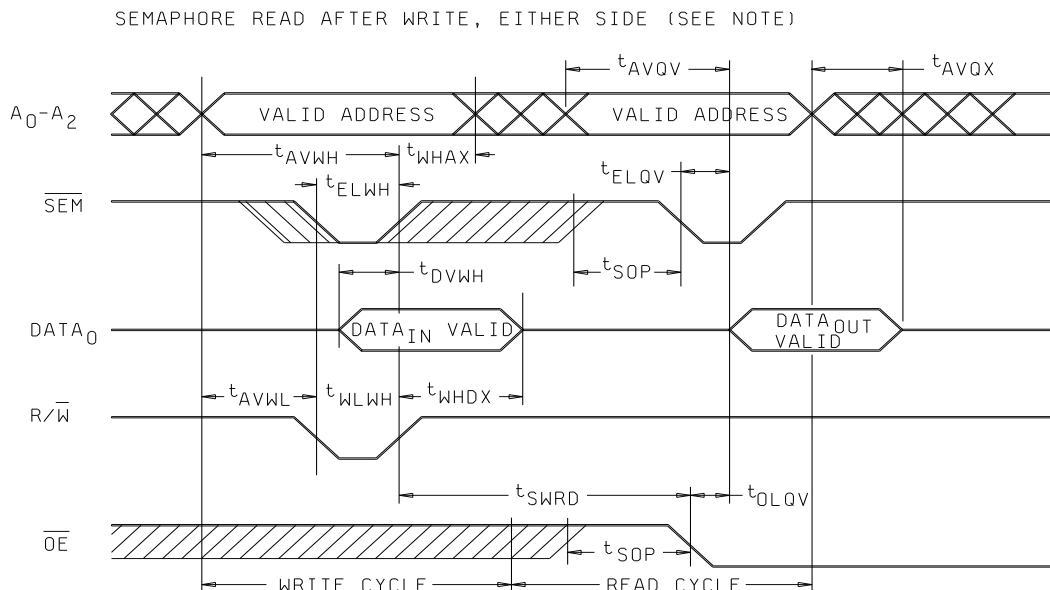


Notes on write cycle:

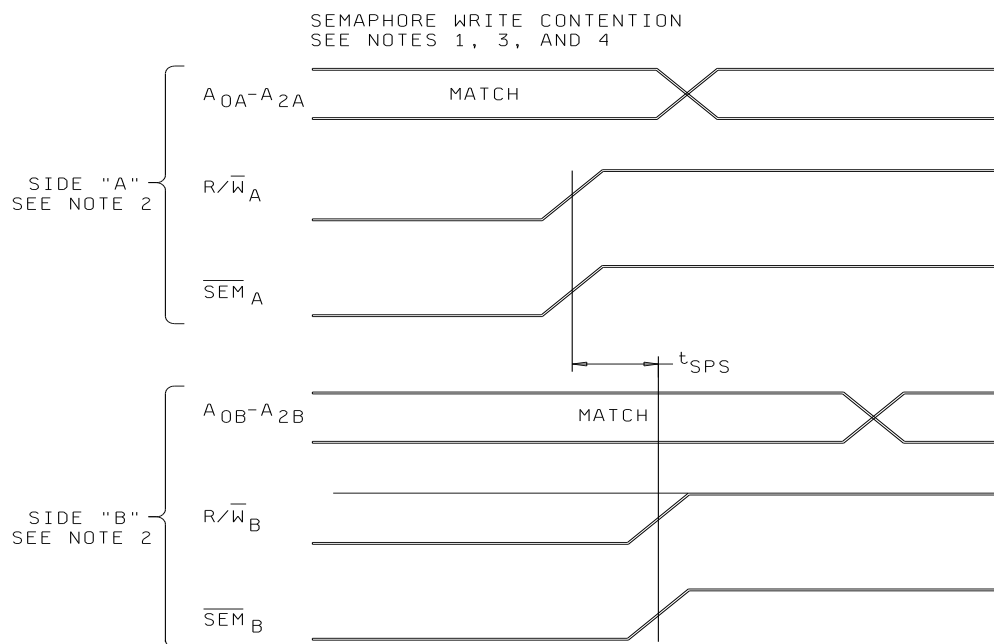
1. R/ \overline{W} must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low \overline{CE} and a low R/ \overline{W} for memory array writing cycle.
3. t_{WHAX} is measured from the earlier of CE or R/ \overline{W} (or \overline{SEM} or R/ \overline{W}) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} or \overline{SEM} low transition occurs simultaneously with or after the R/ \overline{W} low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If \overline{OE} is low during R/ \overline{W} controlled write cycle, the write pulse width must be the larger of t_{WLWH} or ($t_{WLQZ} + t_{DVWH}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DVWH} . If \overline{OE} is high during an R/ \overline{W} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH} .
9. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. t_{EW} must be met for either condition.

FIGURE 5. Timing waveforms - continued.

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Note: $\overline{CE} = H$ for the duration of the above timing (both write and read cycle).

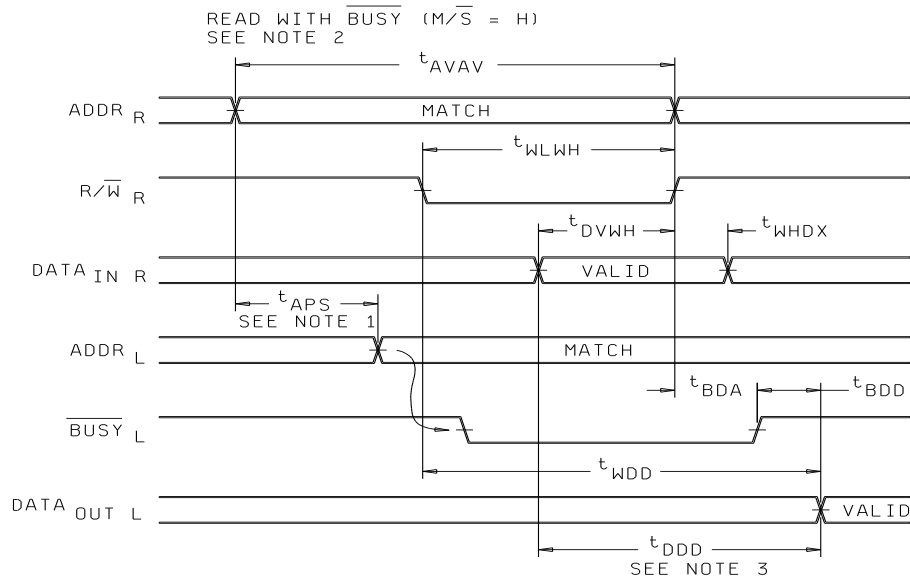


Notes:

1. $DATA_{OR} = DATA_{OL}$, $\overline{CE}_R = \overline{CE}_L = H$, semaphore flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/\overline{W}_A or \overline{SEM}_A going high to R/\overline{W}_B or \overline{SEM}_B going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

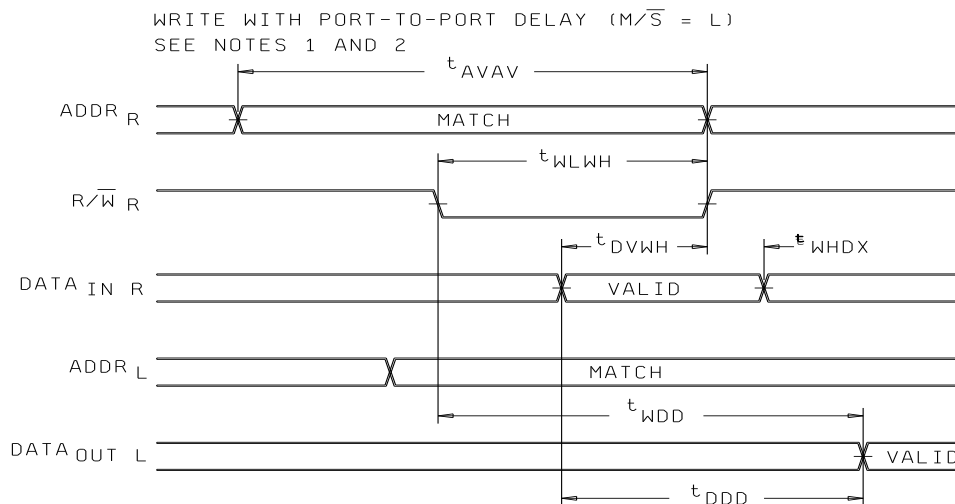
FIGURE 5. Timing waveforms - continued.

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Notes:

1. To ensure that the earlier of the two ports wins.
2. $\overline{\text{CE}}_{\text{L}} = \overline{\text{CE}}_{\text{R}} = \text{L}$.
3. $\overline{\text{OE}} = \text{L}$ for the reading port.



Note:

1. $\overline{\text{BUSY}}$ input equals H for the writing port.
2. $\overline{\text{CE}}_{\text{L}} = \overline{\text{CE}}_{\text{R}} = \text{L}$.

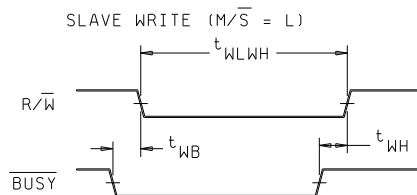


FIGURE 5. Timing waveforms - continued.

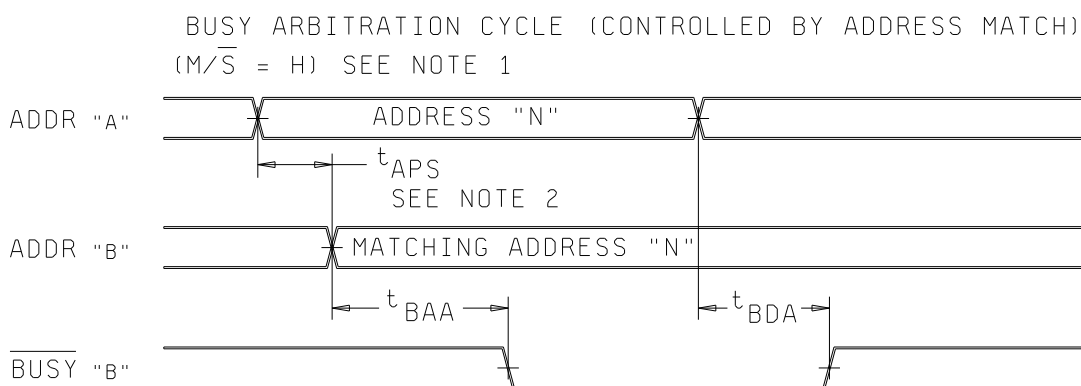
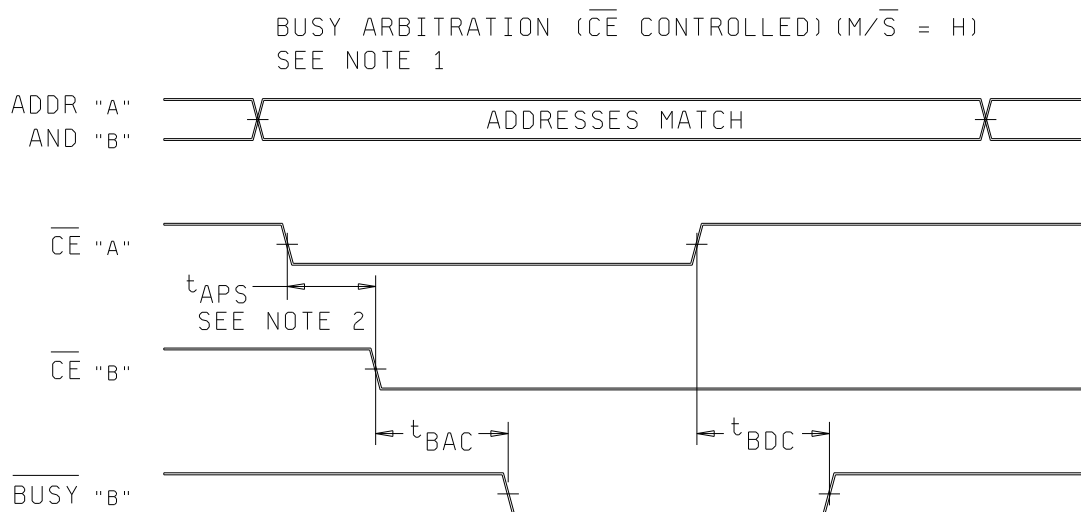
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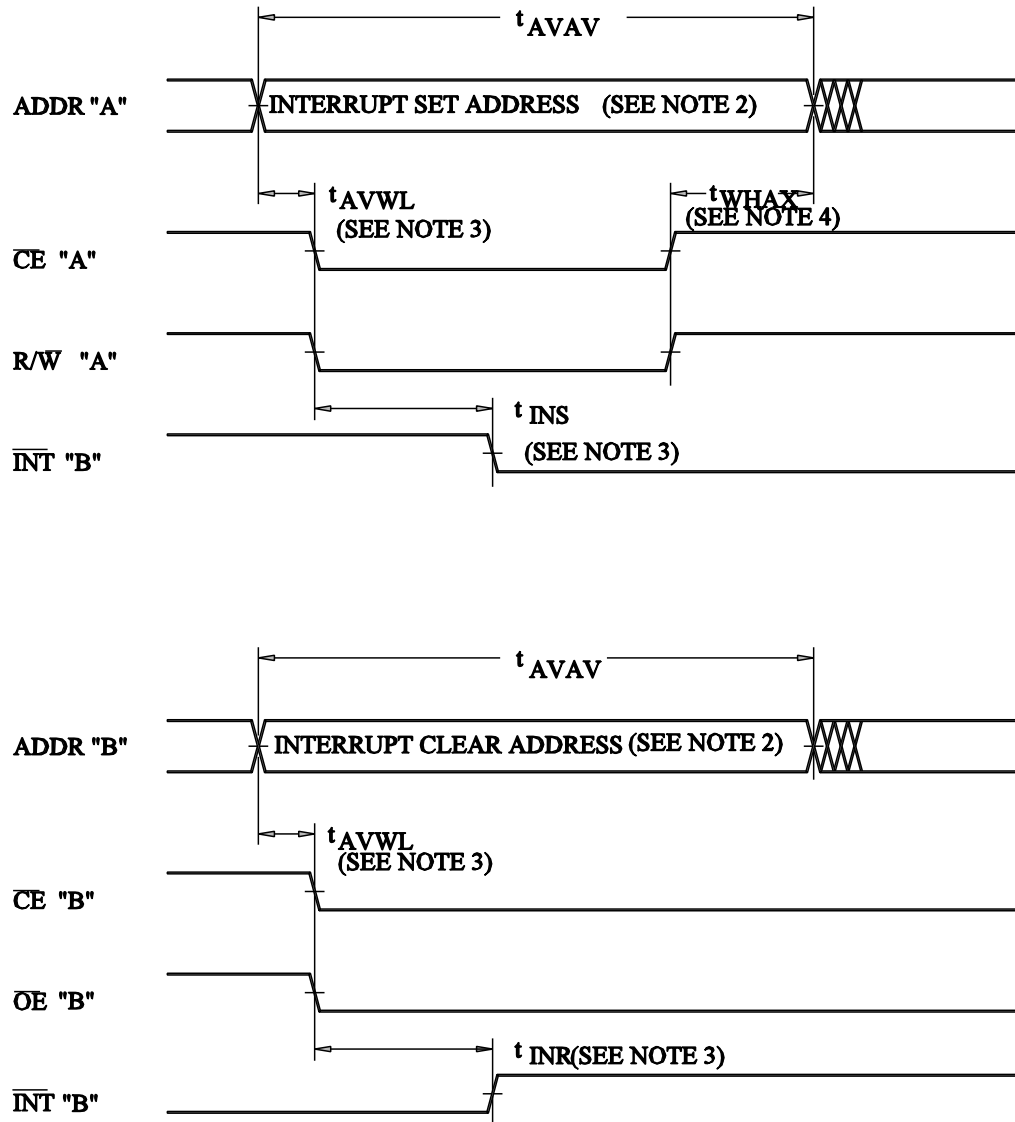
Notes on busy arbitration:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If t_{APS} is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

FIGURE 5. Timing waveforms - continued.

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INTERRUPT TIMING (SEE NOTE 1)



Notes on interrupt timing:

1. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

FIGURE 5. Timing waveforms - continued.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

TABLE IIB. Delta limits at +25° C.

	Device types
Test 1/	All
I _{CC4} standby	±10% of specified value in table I
I _{LO}	±10% of specified value in table I
I _{LI}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

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4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.





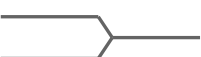
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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

C_{IN}, C_{OUT} -----	Input and bidirectional output, terminal-to-GND capacitance.
GND -----	Ground zero voltage potential.
I_{CC} -----	Supply current.
I_{LI} -----	Input leakage current.
I_{LO} -----	Output leakage current.
T_C -----	Case temperature.
T_A -----	Ambient temperature.
V_{CC} -----	Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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30.3 Algorithm C (pattern 3).30.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-10-10

Approved sources of supply for SMD 5962-91508 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit <u>1/</u> drawing PIN	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9150801MXA	61772	IDT7006S70GB
5962-9150801MYA	61772	IDT7006S70FB
5962-9150802MXA	61772	IDT7006L70GB
5962-9150802MYA	61772	IDT7006L70FB
5962-9150803MXA	61772	IDT7006S55GB
5962-9150803MYA	61772	IDT7006S55FB
5962-9150804MXA	61772	IDT7006L55GB
5962-9150804MYA	61772	IDT7006L55FB
5962-9150805MXA	61772	IDT7006S45GB
5962-9150805MYA	61772	IDT7006S45FB
5962-9150806MXA	61772	IDT7006L45GB
5962-9150806MYA	61772	IDT7006L45FB
5962-9150807MXA	61772	IDT7006S35GB
5962-9150807MYA	61772	IDT7006S35FB
5962-9150808MXA	61772	IDT7006L35GB
5962-9150808MYA	61772	IDT7006L35FB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

61772

Vendor name
and address

Integrated Device Technology
2975 Stender Way
P.O. Box 58015
Santa Clara, CA 95054-8015

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.